Specifications and Transmission Line Practicalities

Introduction

This section focuses on two of industries most widely used balanced transmission line standards, the EIA RS-422 and the EIA RS-485. After reviewing key aspects of these standards, the reader will be introduced to the practicalities of implementing a differential transmission scheme. Finally, several new additions to Texas Instruments EIA product range will be discussed and where appropriate, their application.

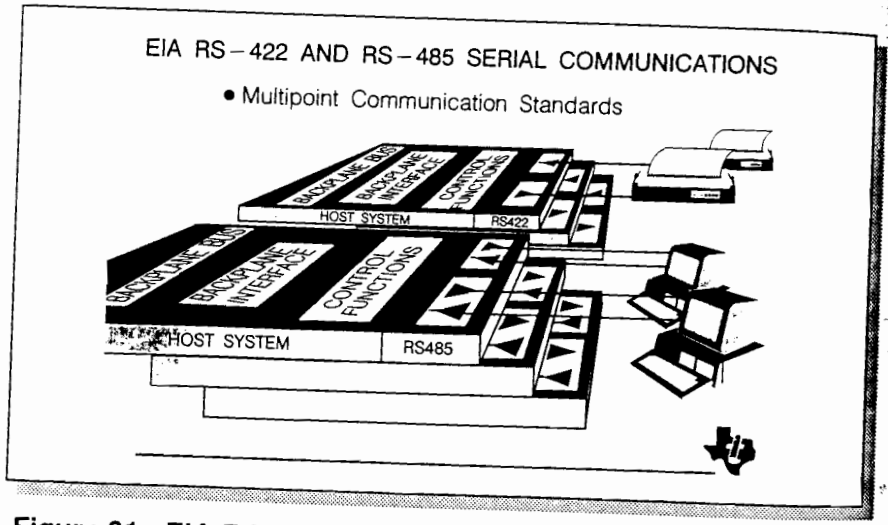


Figure 01 - EIA RS-422 and RS-485 Serial Communications

The Need for Balanced Transmission Line Standards

High speed data transmission between computer system components and peripherals over long distances, under high noise conditions, usually proves to be very difficult if not impossible with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long line system requirements.

RS-422 and **RS-485** are balanced (differential) digital transmission line interfaces developed to incorporate and improve upon the advantages of the current-loop interface and improve on the EIA-232 limitations. The advantages are;

- **Data rate - to 10M baud and beyond**
- **Longer line length - up to 1200 metres**
- **Differential transmission - less noise sensitive**

Application Areas

RS-422 offers a reliable multipoint one way communication. A typical application area is its use in transmitting data from a central computer to multiple remote monitors, printers or stations, such as airport arrival and departure monitors.

RS-485 is an upgraded version of RS-422 extending the number of peripherals and terminals that a computer can interface to, particularly where longer line length or increased data rates are called for. Additionally, RS-485 allows for bidirectional multipoint party line communication and can effectively be used for "mini-LAN" applications, such as data transmission between a central computer and remote intelligent stations. For example, between point of sales terminals and a central computer for automatic stock debiting.

As a result of its versatility an increasing number of standard's committees are embracing the RS-485 as the electrical specification of their standard. Examples include the ANSI (American Nationals Standards Insitute) Small Computer Systems Interface (SCSI).

Notes

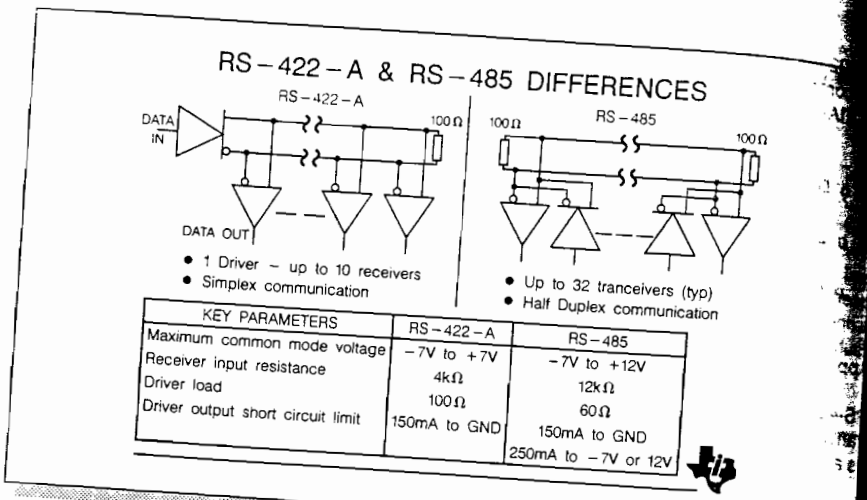


Figure 02 - EIA RS-422-A and EIA RS-485 Differences

EIA RS-422-A

The balanced transmission line standard EIA RS-422 was developed in 1975 to interface a host computer's data, timing or control lines to its peripherals. The standard was revised (RS-422-A) in December 1978 bringing it in line with its present specifications.

A RS-422 line allows for only one way communication (simplex mode) but by using a differential twisted pair transmission media (not specified in std.) and a RS-422 receiver with its minimum 7V common mode voltage capability makes it less susceptible to noise picked up in hostile environments, via the long cables allowed by the standard. Each driver can drive up to 10 receivers. The specification in the standard places no restrictions on minimum or maximum operating data rates but rather on the relationship of transition speed to a unit interval. However, data rates up to 10M baud are supported and a line length up to 1200 metres is given as guide-line, but not at the maximum data rate.

When operating at low data rates (below 200k baud), or at any speed where the ratio of the driver's output rise time to the one-way propagation delay time of the cable exceeds ten, the cable will not act as a true transmission line and therefore termination is not absolutely necessary. Under all other conditions, the cable loading can no longer be considered as a lumped parameter but must be considered as a transmission line.

The characteristic impedance of twisted pair cable is a function of frequency and cable type, however typical twisted pair cable impedances lie in the range of 100Ω to 120Ω. A

mination resistor with an impedance similar to the cable's characteristic impedance should y be connected at the furthest end of the cable.

A RS-485

e Increased use of balanced data transmission lines in distributing data to several system mponents and peripherals over relatively long lines brought about the need for multiple ver/receiver combinations on a single twisted pair line. Hence, an upgraded version of EIA S-422-A , named EIA RS-485, was introduced in 1983.

S-485 takes into account RS-422 requirements for balanced-line data transmission plus dditional features allowing for multiple drivers and receivers. The guide-lines for data ansmission speed, cable lengths and media are the same as for RS-422.

he Differences

he differences between the RS-485 standard and the RS-422 standard lie primarily in the eatures that allow reliable multipoint communications.

Driver features

1. One driver can drive as many as 32 unit loads (one unit load is typically one passive driver and one receiver).

2. The driver output, off-state, leakage current shall be 100μA or less with any line voltage from -7V to +12V.

3. The driver shall be capable of providing a differential output voltage of 1.5V to 5V with common-mode line voltages from -7V to 12V.

4. Drivers must have self protection against contention (multiple drivers contending for the transmission line at the same time).

Receiver features

1. High receiver input resistance, 12kΩ minimum.

2. A receiver input common-mode range of -7V to 12V.

3. Differential input sensitivity of ±200mV over a common-mode range of -7V to 12V.

Notes

Line Drivers, Receivers and Transceivers for RS-422 and RS-485

Texas Instruments has a wide range of devices supporting these standards as specified in the following tables:

APPLICATION	DEVICE FUNCTION	DEVICES PER PACKAGE	DEVICE TYPE
EIA Standard RS-422-A	Drivers	2	SN75158
			SN75159
			SN75ALS191[1]
			µA9638C
		4	AM26LS31C
			AM26C31[2]
			MC3487
			SN75151
			SN75153
			SN75ALS192[1]
			SN75ALS194[1]
	Receivers	2	SN75146
			SN75157
			µA9637A
			µA9639C
		4	AM26LS32A
			AM26C32[2]
			MC4386
			SN75ALS193[1]
			SN75ALS195[1]

APPLICATION	DEVICE FUNCTION	DEVICES PER PACKAGE	DEVICE TYPE
EIA Standard RS-485 and EIA Standard RS-422-A	Drivers	4	SN75172
			SN75174
	Receivers	4	SN55173
			SN75173
			SN75175
	Transceivers	1	SN65LBC176[2]
			SN75LBC176[2]
			SN65176B
			SN75176A[1]
			SN75176B
			SN65ALS176[1]
			SN75ALS176[1]
			SN75ALS176A[1]
			SN75ALS176B[1]
			SN75177B
			SN75178B
			SN95176B
			TL3695
		3	SN75ALS170
			SN75ALS171
	Drivers / Receivers	1 / 1	SN75179B
			SN65ALS180[1]
			SN75ALS180[1]
		2 / 2	SN751177[1]
			SN751178[1]

NOTES: 1. New product release
2. Product under development

Detailed Description of Key RS-485 Specifications

The following text describes in some detail the key specifications embraced by the RS-485 standard.

Notes

Generator (Driver Characteristics)

The open circuit test (left in figure). Used to define the differential and single-ended voltage range for the logic states as follows:

For either logic or binary state, the magnitude of the differential voltage, V_o measured between the two driver output terminals shall be not less than 1.5V and not more than 6V; and the magnitude of V_{oa} and V_{ob} measured independently between each generator output terminal and generator circuit ground shall be not more than 6V.

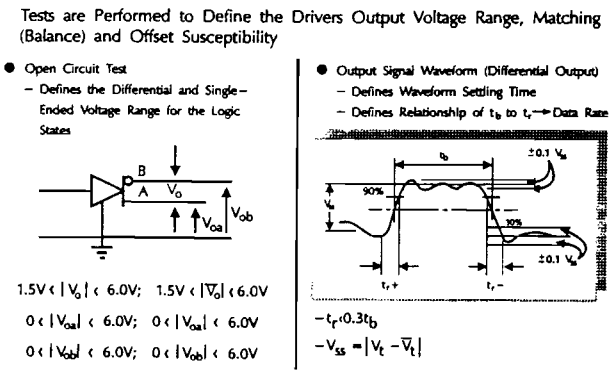


Figure 2a- Generator (Driver Characteristics)

The output signal waveform - differential output (right in figure). This defines both the waveform settling time and the relationship between the waveform unit interval (t_b) and the waveform rise time (t_r). It is this relationship which sets the limit on the data rate achievable using the RS-485 standard. (Note, the same rule applies for the RS-422 specification but with a relaxed ratio, see previous section). The differential output voltage measured across the test load, 54Ω in parallel with 50pF, should have a monotonic transition between the binary states. Thereafter, the signal voltage shall not vary by more than 10% from the steady state value of V_{ss} (the differential voltage between the two states of the generator output), until the next binary transition occurs. The instantaneous magnitude, V_t and $\overline{V_t}$ of either binary state shall not exceed V_{ss} or 5V.

RS-485 defines the maximum data rate of a device in terms of the transition time, t_r relative to one unit interval, t_b. If the transition time for a device is known then the maximum operating data rate, fb for RS-485 conditions can be calculated as follows:

$$t_r = 0.3\ t_b \quad \text{or} \quad t_b = t_r/0.3;$$

For example, the SN75ALS176 has a specified maximum transition rise time (t_r) of 8ns. At worst case the maximum data rate would be:

$$f_b = 0.3/(8\text{ns}) = \underline{37\text{M baud.}}$$

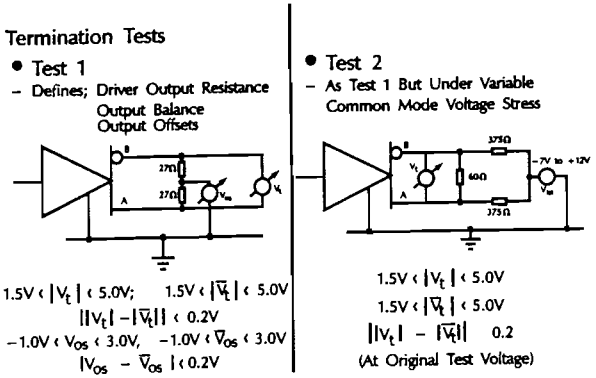


Figure 2b- Generator Tests Continued

There are two termination tests carried out; Test one defines the output resistance, balance and offsets of the driver. With the test load as shown, the magnitude of the differential voltages, V_t and the offset voltages, V_{os} should be as specified. The balance, difference between the magnitudes of the differential outputs, of the driver should be within 200mV. Where the offset, or common-mode output, voltage of the driver should not be less than -1V and not more than 3V.

Test two is used to measure the magnitude of the differential voltages, Vt, under worst case common-mode signal (-7V to 12V) conditions. The circuit is loaded as shown on the righ hand side of the figure and should yield the results as stated.

Notes

Receiver Characteristics

The two main tests carried out on the receiver are the sensitivity test and the balance measurement used to give an indication of the receiver's ability to reject common mode signals.

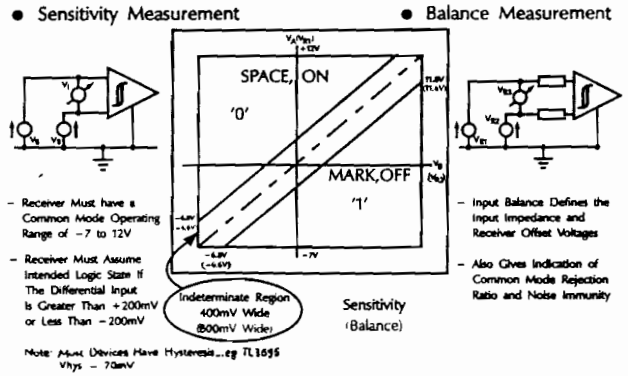


Figure 2c- Receiver Characteristics

Sensitivity and Balance Measurements

Sensitivity measurements. The maximum range of input voltages appearing at the receiver input terminals measured with respect to receiver common shall be between -7V and 12V. For any combination of receiver input voltages within the allowed range, the receiver shall assume the intended binary state with an applied differential input voltage of +/-200mV or more. To avoid faults from noise on slow rising/falling signals, receivers usually have hysteresis incorporated in to their input stages, E.g. TL3695 Vhys = 70mV.

Input balance measurements. This defines the input impedance and receiver offset voltage, and gives an indication of how well a device rejects common-mode signals. With a test configuration as shown, a differential signal of +/-400mV is applied through two equal valued (1500 Ohm /(number of unit loads) series resistors. With this signal applied, the receiver output shall remain in the intended binary state throughout the -7V to 12V common-mode range.

Fault Conditions

The RS-485 standard has been designed with the realities of long distance and high data rate communication in mind. Therefore the standard takes great care in ensuring that adequate fault protection and robustness is built into devices claiming RS-485 conformance. Detailed in the following figure are just some of the tests used to ensure device robustness.

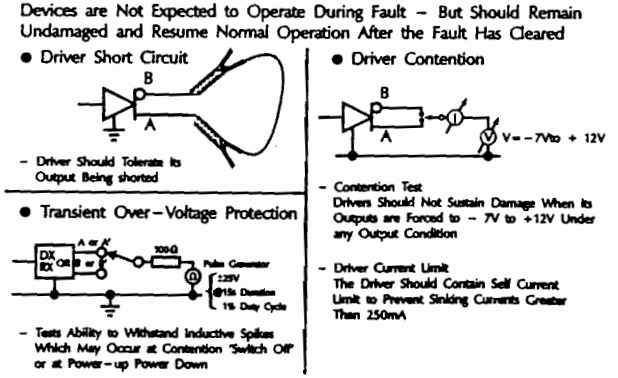


Figure 2d - Fault Conditions

However, it should be noted that even with the precautions taken by the RS-485 standard some applications demand even greater levels of fault protection and tolerance. Excessive and damaging voltage (more than +/-25V) stress on the receiver inputs can be clamped with appropriate circuitry - while excess common-mode voltage exceeding the maximum specified range (-7V to 12V) by the standard, can usually be avoided by effective grounding techniques and choice of shielded twisted pair cables as transmission media.

Notes

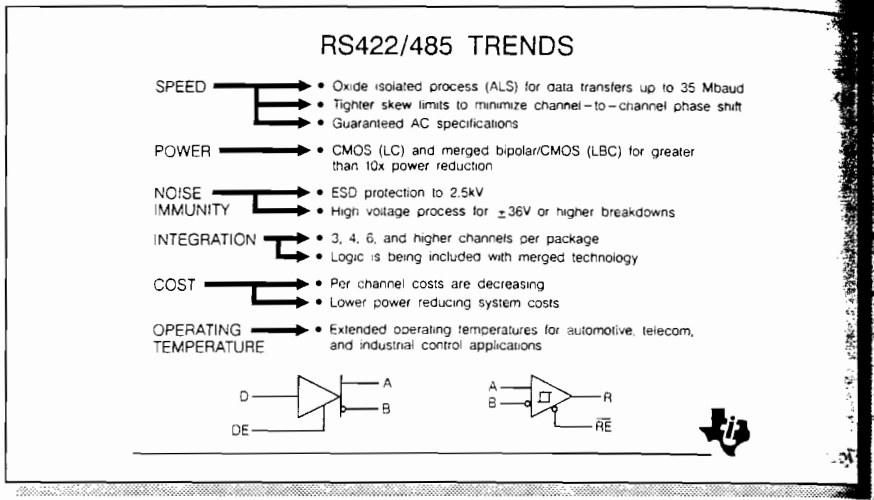


Figure 03 EIA RS-485 /422 Product /Application Trends

Many propriety systems designers are beginning to recognise the inherent advantages of a balanced, differential, transmission scheme over the single ended interface. Such advantages are higher noise immunity, lower noise emissions and improved signal quality. These facts are also not lost on independent standards committees which are starting to embrace RS-485 as the electrical part of their overall specification. Furthermore those systems not following the RS-485 specification verbatum are recognising the virtues of Texas Instruments range of differential driver/receivers, particularly the high speed/low power ALS options.

Representatives of those standards bodies employing a differential transmission scheme can be found in most industries, some examples are listed below;

i) **Computer;** The ANSI-X3T9.2-1986 Small Computer Systems Interface (SCSI)
ii) **Computer;** ANSI X.3129-1986 Intelligent Peripheral Interface (IPI)
iii) **Automotive multiplex Wiring;** CAN, VAN and SAE J1850
iv) **Telecommunications;**
v) **Factory Automation;** P-Net (A derivative of Field bus)

Each one of these application areas makes its own demands on the processing technology used. Examples of these demands are guaranteed AC specifications and increased data rate capability. In particular, tighter skew specifications are needed for both telecommunication and computer applications, however the interpretation of skew can differ. For example, telecommunication applications are more concerned with device skew, that is the difference between the positive and negative edges of the differential output voltage. A low skew value in this case would represent a lower likelihood of noise radiation. For the

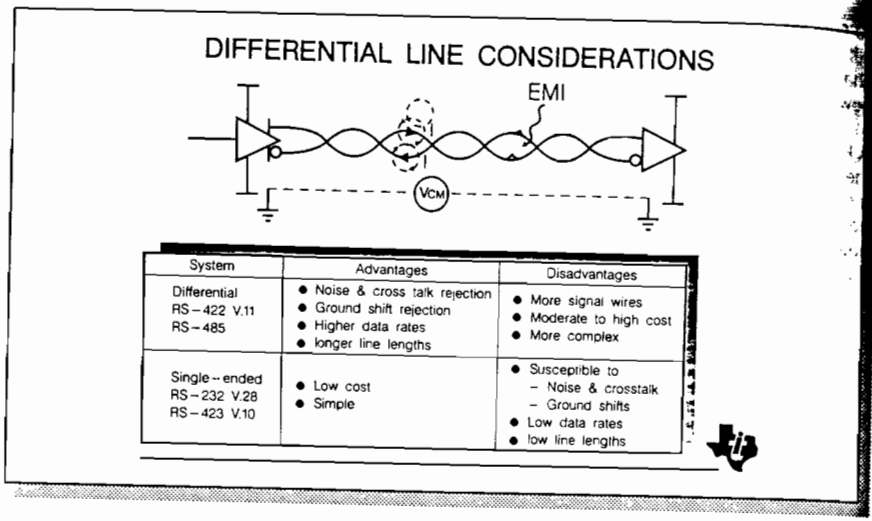
omputer application, SCSI, a low bus skew is required. In a SCSI there can be as many 18 ifferential lines, obviously for timing purposes it is desirable to have low skew between each hannel. For these types of applications a high speed bipolar process like the advanced low ower scchottky would be required.

key requirement across most application areas is low power consumption, particularly with he emergence of battery backed or operated equipments. This requires a low power echnology, for example CMOS. However although fine for controller applications, CMOS is ot generally suitable for line drive/ receive functions, here a more robust technology is eeded, for example, a bipolar or merged technology like Texas Instruments' LinBiCMOS combination of analogue bipolar and analogue CMOS).

Due to the increasing use of differential systems, particularly in electrically hostile nvironments, increased common mode voltage ranges and low susceptibility to ESD Electro-Static Discharge) damage is required. Furthermore, extended temperature ranges re required particularly in automotive applications where the line drive/receive functions may e located under the car bonnet (hood). All new devices in Texas Instruments' range of line rivers and receivers contain temperature range options for both commercial, 0° C to 70°C nd industrial, -40°C to 85°C. Some devices like the SN65076 have been designed especially for automotive applications by offering a -40°C to 105°C temperature range.

One final demand made by all types of equipment is for increased integration. Designers are requiring increased functionality from semiconductor chips and, perhaps an even more importantly require that these chips be less expensive than the solution(s) they replace.

Notes



System	Advantages	Disadvantages
Differential RS–422 V.11 RS–485	• Noise & cross talk rejection • Ground shift rejection • Higher data rates • longer line lengths	• More signal wires • Moderate to high cost • More complex
Single–ended RS–232 V.28 RS–423 V.10	• Low cost • Simple	• Susceptible to – Noise & crosstalk – Ground shifts • Low data rates • low line lengths

Figure 04 - Differential Line Considerations

A differential communication system requires the use of two 'signal carrying' wires between driver and receiver, such that the signal current flows in opposite directions in each wire. The net effect of doing this is that the receiver is only concerned with the *difference* in voltage between the two wires. The absolute value of the d.c common mode voltage of the two wires is not important. In practice, drivers and receivers have a finite common mode voltage range within which they can operate.

The use of a differential communications interface allows data transmission at high rates and over long distances to be accomplished. This is because effects of external noise sources and crosstalk effects are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is insensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same argument, a change in the local ground potential at one end of the line will appear as just another change in the common mode voltage level of the signals. The differential output voltage to the line will also provide a doubling of the driver's single-ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost, but provides superior performance when data is to be transmitted at high rates over a long distance.

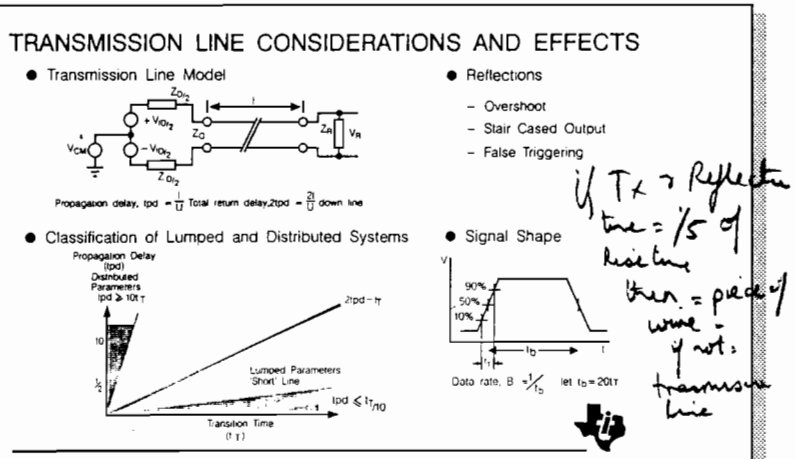


Figure 05 - Transmission Line Considerations and Effects

Before design of a digital data link can take place application constraints and an understanding of the signal's characteristics must be understood. More specifically, a method of identifying the class of data link, and any special design techniques required must be made.

A digital data link can be classed in two modes;

i) A transmission line (distributed parameter model)
ii) Short wire (lumped parameter model).

A distributed parameter model considers the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections making up the line. The result is that a transmission line is said

Notes

to have a characteristic impedance, Z_0, which is independent of distance along the line and represents the voltage and current relationship for a wavefront at any point as it travels along the line.

The transmission line will always consist of two conductors, with the current flowing in opposite directions in each of the conductors. In the single ended case, one of these conductors is the ground wire.

The speed that a pulse travels at along a transmission line approaches that of the speed of light. The type of cable used will provide the limit to the actual speed.

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings. If the signal starts to change at the driver's output at one end of the line, the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the driver terminals. If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system. A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated. If the rise time , t_r, of the signal is much less than the round trip propagation delay, $2t_{pd}$, of the signal from driver to receiver and back to driver, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given by allowing 10 one way propagation delays, t_{pd}, to occur during the transition edge time.

When the cable is operating like a transmission line, extra loads in the form of drivers and receivers can be added, providing that they do not cause too great a shunting effect on the line. These extra loads, if evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. The extra devices will decrease the line impedance and reduce the speed of the signal along the line.

In the case of the lumped parameter model, the line tends to represent a pure fixed load to the driver device. For example, the capacitance of the line will be modelled as a fixed value which effectively limits the output voltage slew rate of a driver device that can supply a finite amount of current to the line.

Line Termination

It is generally good design practice to terminate the ends of lines which are classified as transmission lines. Here the golden rule is to match the impedance from the source of the driver to the characteristic impedance of the cable, and from the cable to the characteristic impedance of the receiver. If there is an impedance discontinuity at any junction, then the signal will be reflected from the mismatch. This will lead to signal distortion which in turn leads to either a falsely triggered receiver or excessive propagation delay. Calculation of a suitable value for this termination value will be dealt with later in this section whilst a more detailed discussion can be found in the glossary section.

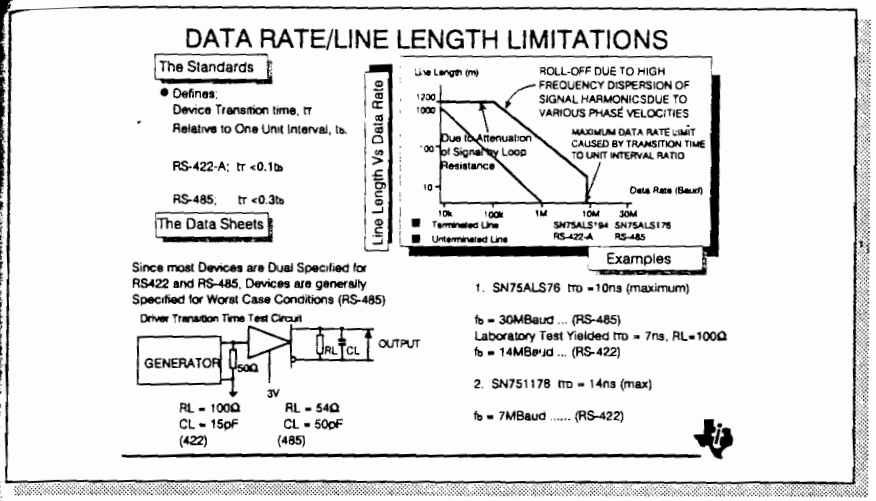


Figure 06 - Line Length and Data Rate Limitation

Most application areas will demand some kind of compromise between the line length used and the data rate required, particularly if distortion in its many guises is to be avoided. A first, all important, step in understanding what compromises are necessary is to recognise the various forms of distortion and why they occur.

No transmission line is perfect, even by sending current down the line some voltage drop will occur due to the resistive nature of the line, this in its most simplistic form is distortion. This is compounded when longer line lengths are used where the attenuation from source to destination can cause quite severe distortion. This places a limit on the line length even at low data rates as shown in the top right hand corner of the figure.

A typical cable of 24 SWG can have a series resistance of 80 Ω per km, and so the line length will be limited to the order of 1200m (series resistance equals the line's characteristic impedance).

Notes

The Standards

Another limitation of system performance are the speed limitations of the line dri elements themselves. No device, no matter what technology used, will have zero propaga delays and transition times. The trick is to ensure that any delay introduced by these dev is insignificant in comparison to the line propagation delay. To ensure the device does introduce distortion, ie to maintain signal shape, it is good design practice to set a r between the unit interval, t_b, and the transition rise time, t_T .This limitation is often specified the standard being used. For RS-422-A the ratio of t_T to t_b is 1: 10, and for RS-485 1:3.

The Data Sheets

Many devices within Texas Instruments' range are specified for both RS-422 and RS-48 operation. The differing specifications of relating t_T to t_b between the standards makes a understanding of data rate capability for RS-422 operation difficult to ascertain, since thes devices are tested to the worst case conditions of the RS-485 specification. That is, th driver output is driven into a resistive load of 54Ω in parallel with a capacitive load of 50pF

An example of such a device is the SN75ALS176 which can be used for both RS-422 & RS-485.

Examples

1. **SN75ALS176B** has a differential-output transition time t_T of 10ns(Max).

Therefore; $t_b = 3.33 \times 10x10^{-9} = 33.3ns$ giving a minimum theoretical frequency o **30Mbaud.**

As the data sheet specifies a minimum t_T = 5ns the maximum theoretical data rate could be as high as 60 Mbaud.

Using the RS-422 data rate test for this devices does not give a clear picture as the standard requires a lighter load to be applied. However, laboratory test using the RS-422 load gives a t_T for the ALS176 of 7ns (RS-485 load = 14ns) indicating a RS-422 data rate of 14Mbaud.

2. **SN75ALS194** has a differential-output transition time t_T = 14ns(Max). Since this device is specified solely for RS-422 we can clearly calculate the minimum theoretical data rate.

Therefore; $t_b = 10 \times 14x10^{-9} = 10 \times 14x10^{-9}$ giving a minimum theoretical frequency of **7Mbaud.**

Again a more aggressive data rate could be achieved if the typical specified value for t_T = 8ns was used. Giving a typical frequency of 12.5 Mbaud.

her Effects

her effects acting upon the transmission line are due to phase distortion introduced on the iver's transition edges. The high speed edges, necessary for high speed systems, have high frequency harmonic content. The inductive and capacitive (and resistive) nature of e line introduces delay and distortion into these harmonics. This in turn reduces the clarity the signal being sent down the line, thus increasing the probability of error.

his effect is normally measured using eye patterns which measure the jitter and distortion in e signal being sent down the line. It is this effect that causes the predominant reduction in ata rate as the line length increases. Another limitation can be caused by incorrect rmination of the line, causing reflections. These reflections can cause errors due to loss of ming information.

n conclusion, distortion and thus data integrity is a function of signal rise time and line ttenuation. Signal rise time and attenuation are often quoted in manufactures data, and can e used to determine the line distortion.

A Discussion of Skew

When driving the line at high speeds the effects of the driver and receiver on the system become more apparent. The size of the delays relative to the unit interval will increase, meaning that asymmetries in the edges can cause extra distortion on the output to the line.

Using differential line systems, the delays through the driver and receiver have different meanings. This is because the driver is really a single ended input to differential output converter, while the receiver is a differential input to single ended converter.

When discussing propagation delays through the driver, two possibilities arise; the propagation delay from the input to one output and the other output (single ended) and also the propagation delay from the input to the differential output (differential).

The single ended propagation delay is normally measured between the input going through 1.5V and the output going through 1.5V, while the differential propagation delay is measured from the input going through 1.5V and the differential output going through its mid-voltage, (in a balanced line 0V across the line).

Notes

These propagation delays effectively displace the signal on the line in time, but do not distort it, however, differences in the delays from output A going high and output B going to output A going low and output B going high does cause distortion. The differences between these are termed as the skew in the output. For a single ended measurement it is termed ***Propagation Skew***, while for the differential measurement it is termed ***Differential Skew***.

The main effects of propagation skew are that the differential transition edges can be stretched out and that they can become flat around the threshold region of the receiver, i.e. at the common mode voltage of the line. This gives the system a lower noise immunity and can increase the radiated RFI and sensitivity.

The main effect of the differential skew is the asymmetry caused by different differential propagation delays causing one state to be longer than the other state.

The propagation skew is specified on the older differential line drivers, while differential skew is specified on the more modern devices such as Texas Instuments' SN75ALS176.

The receivers are tested on the propagation skew. With one input tied at a reference voltage and the other toggled, giving a single ended propagation delay. The skew in this delay will also cause extra distortion to the signal, especially its timing information, as the periods can be further distorted.

Practical Considerations

Having reviewed some of the key issues involved in implementing a high speed differential data link, practical ways in which to overcome some of the problems encountered are now discussed.

The first areas of concern are how to make connections to the line, how and where the line should be terminated and into what value?.

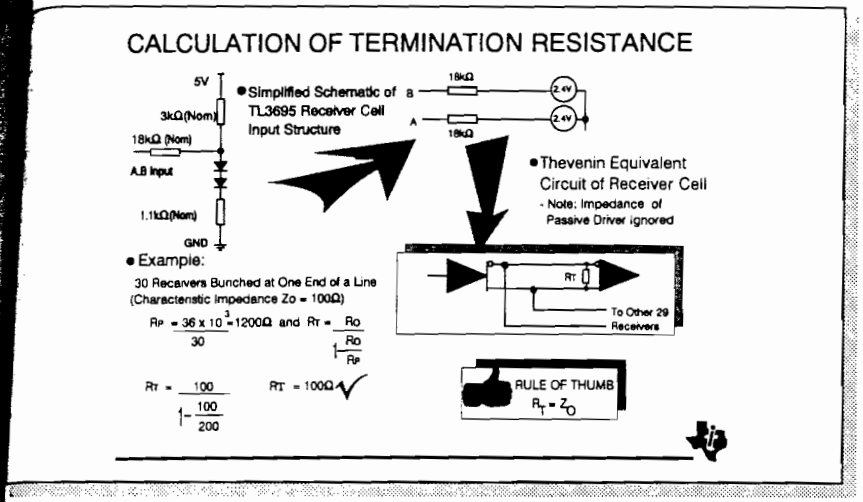


Figure 07 - Calculation of Termination Resistance

For better performance, the transmission line needs to be terminated by a resistor of a value close to its characteristic impedance. One question that immediately arises is the value of terminating resistance required if the line is loaded by other receivers. More specifically, does the receiver's input impedance have any effect?, especially when many receivers may grouped together at the far end of the line. The following text sets out to prove that for the majority of applications the loading effect of receiver stations can be ignored and as a rule of thumb (working approximation) the value of R_T should equal the characteristic impedance of the line.

In fact, the characteristic impedance varies very little with respect to the physical dimension of the cable. For example a wire over-ground transmission line with a wire diameter equal to the diameter of an electron and a height above the ground plane of 500,000Tm (50 light years) has a characteristic impedance, Z_O, of 3000Ω.

Notes

Each input of the receivers has a nominal input impedance of 18kΩ feeding into a dc transistor- resistor biasing network, this is equivalent to an 18kΩ input resistor tied to common mode voltage source of 2.4V. -It is this configuration which provides the large common range of the receiver required for RS-485 systems!.

Due to the fact that the each input is biassed to 2.4V, the normal common-mode voltage of balanced RS-485 systems, the 18kΩ resistors on the inputs can be taken as being in series across the input of each individual receiver.

If thirty such receivers are placed close together at the end of the line, they will tend to react as thirty 36kΩ resistors in parallel with the termination resistor. This overall effective resistance will need to be close to the characteristic impedance of the line.

The effective parallel receiver resistance, R_P, will therefore be equivalent to;

$$R_P = 36 \times 10^3 / 30 = 1200\Omega .$$

While the termination resistor, R_T, used will be equal to;

$$R_T = R_O / [1 - R_O/R_P] .$$

Thus for a line with a characteristic impedance of 100Ω, the termination resistor R_T should be:

$$R_T = 100/[1 - 100/1200] = 110\Omega$$

Since this calculated value is within 10% of the line characteristic impedance the value chosen for the line termination resistor, R_T, will normally be equal to the characteristic impedance, Z_O.

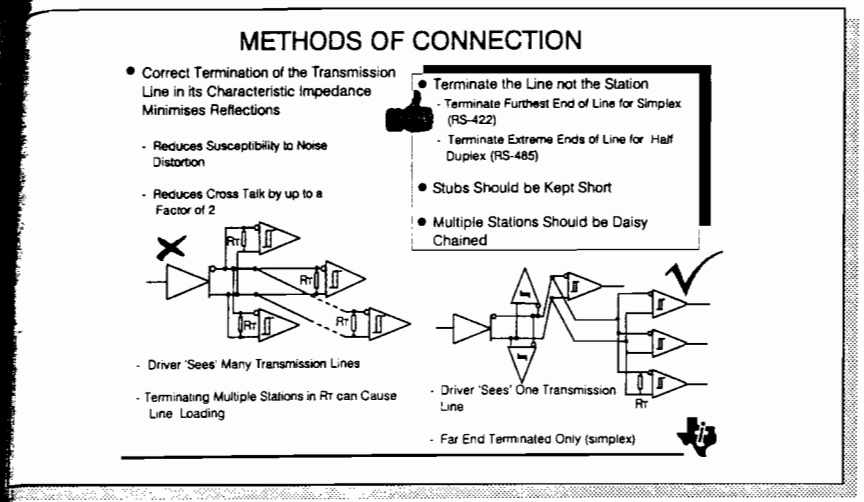


Figure 08 - Methods of Connection

Methods of Connection

The way in which stations are connected to the line needs careful consideration. Furthermore methods of line termination and device positioning must be considered. There are two basic methods of connection;

i) **The star connection**
ii) **The daisy chain connection**

Considering the star connection, the transition edge from the driver will be loaded by a group of separate transmission lines, rather than one. Each transmission line boundary will cause a change in impedance resulting in reflections.

Notes

Another situation to avoid is the termination of multiple stations, since this could excessively load the driver. Termination at the extreme ends for RS-485 (half duplex) and far end only for RS-422 is recommended. Normally stubs (taps of the main line) should be kept as short as possible so not to appear as transmission lines themselves.

The recommended method is to use the daisy chain, a configuration where the transmission line continues from one receiver to the next and only the last receiver on the chain is terminated. This means that the transmission line and hence the driver will see one continuous transmission line with only one termination resistor. Each tap-off will in effect be a stub, but in this case they will not be all grouped together and will be kept very short to reduce their effect.

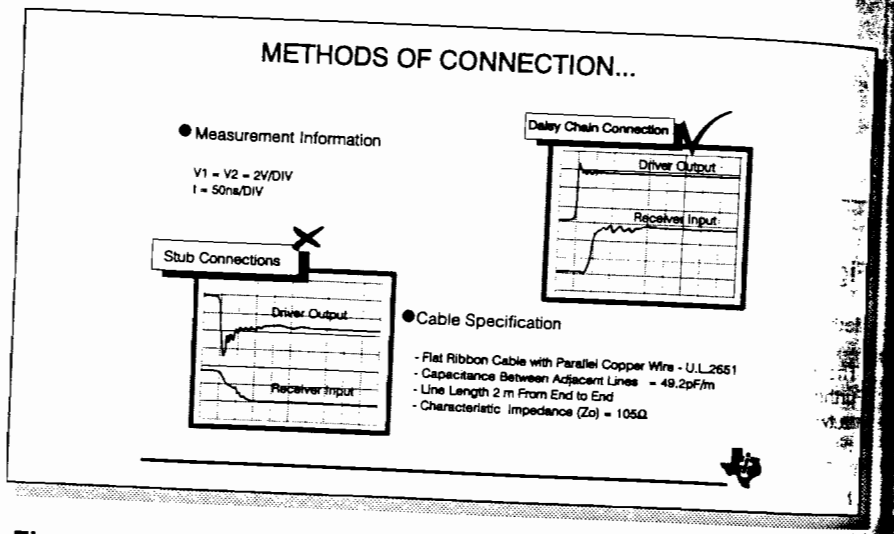


Figure 09 - Methods Of Connection...

Comparing the Quality

The figure shown, further confirms the need tor keep stub lengths short and the use of correct termination techniques by comparing the effect on signal quality for the daisy chain and star method of connection.

In both instances exactly the same application scenario was used as was the same cable specification. The cable used was a flat ribbon cable with parallel copper wire conforming to U.L. specification 2651. Connections were made as shown in the previous figure and the total cable length from source to destination was 2 m.

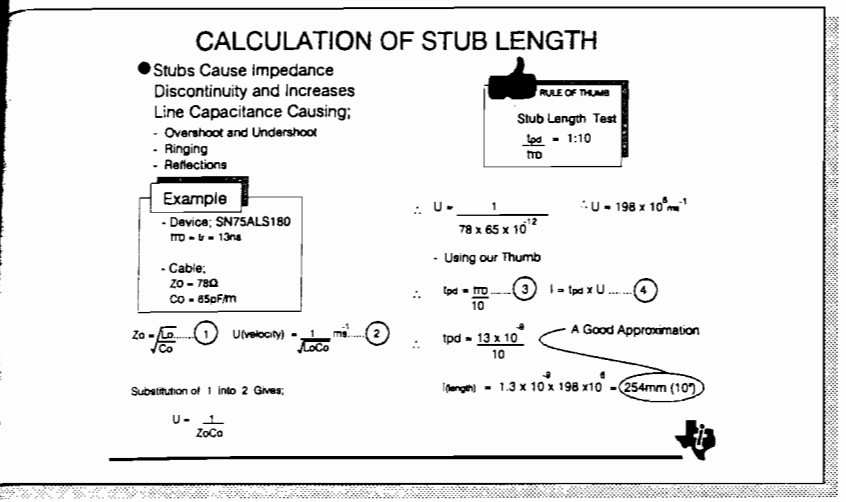


Figure 10 - Calculation of Stub Length

In the earlier section a rule of thumb was developed which stated that if signal distortion is to be avoided, all connections to the main line must be kept as short as possible. Distortion in this context could be both amplitude and phase distortion - leading to reflections amongst other undesirable factors.

These connections are usually termed stubs. A stub is a connection to the transmission line from either a driver or a receiver . However, even when short in comparison to the length of the main transmission line it too could exhibit transmission line effects. Any connection to the line will cause an impedance discontinuity, leading to reflection at the stub/transmission line boundary.

To minimise these effects the stub should be kept as short as possible, so that the stub is seen as a lumped (non transmission line) rather than a distributed (transmission line) load to the line.

Notes

How Short is Short ?

It has been described earlier that a pair of cables will act as a transmission line if the rou
trip propagation delay, t_{pd} ,is more than 5 times the transition times of the driver, t_T. Th
converse is true if the line is not to operate as a transmission line but as a lumped parame
model. This forms the basis of the stub length calculation given below.

The figure shows a calculation for determining the maximum length of the stub. The rule o
thumb that the transition time of the pulse sent down the line should take ten times th
time taken for the pulse to propagate to the end of the stub. Rsulting in any reflections being
incorporated into the transition edge.

From this basis, the length of a stub can be calculated using the cable and driver parameters.

The pulse speed down the line, U, equals the reciprocal of the product of the line impedance
and line capacitance, both of which are normally specified for the cables used.
The propagation delay down the stub should be at the most one tenth of the transition time of
the pulse. These facts can be brought together to give the length of the stub, l_S , as;

$$l_S = t_{TD} / (10)$$

Using the SN75ALS180 and its transition time of 13ns, a cable with a characteristic
impedance of 78Ω and line capacitance of 65pF, gives a maximum stub length of 254 mm or
ten inches.

The main effect in this case will be a slight increase in the capacitance loading of the line.

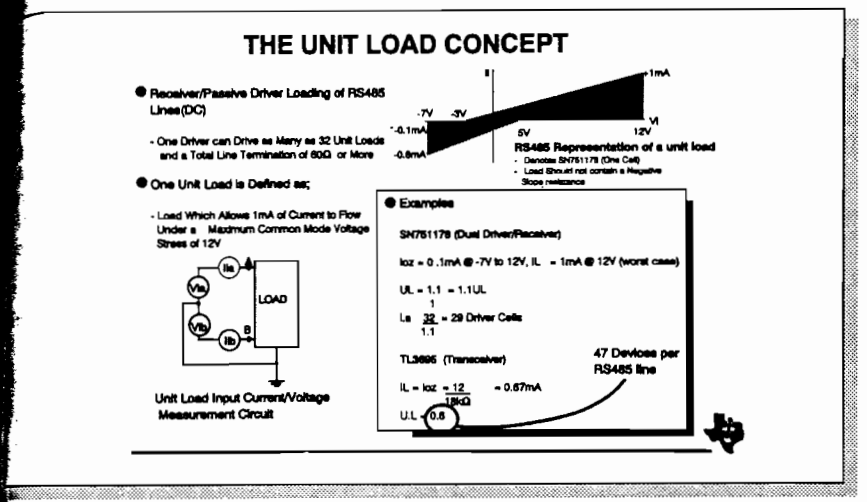


Figure 11 - The Unit Load Concept

Line Loading Considerations

One final consideration needed to implement a digital data link is the number of driver/ receiver elements that can be connected to the line. This is now discussed;

The Unit Load Concept (RS-485)

The maximum number of drivers and receivers that can be placed on a single communication bus depends upon their loading characteristics relative to the definition of a unit load (U.L). RS-485 recommends a maximum of 32 unit loads per line.

One U.L (at worst case) is defined as a load that allows 1 mA of current under a maximum common-mode voltage stress of 12 V . The loads may consist of drivers and/or receivers but

Notes

does not include the termination resistors, which may present additional loads as low as 60 total.

The first example shows a unit load calculation for the dual SN751178 driver/receiver which offers a unit load value of 1.1 U.L - meaning 29 such devices could be connected on one line. In the second example the TL3695 transceiver is used. Since this device is internally connected as a transceiver, ie driver output and receiver input connected to the same bus, it is difficult to obtain separate driver leakage and receiver input currents. For this calculation reference is made to the receiver input resistance, 18kΩ, giving a transceiver current of 0.6mA. This can be taken to represent 0.6 U.L. which will allow upto 47 devices to be connected to the line.

Obviously it may be possible to connect more devices than the RS-485 recommendation, but this is at the designers risk.

The graph in the top right corner of the figure is used to define the boundaries of the unit load and works by superimposing the voltage and current characteristics of the load upon a reference trace. A line from - 3 V is drawn at a tangent to intercept receiver input current at the 12 V point. Similarly, a line is drawn from -7 to intercept the driver leakage current at the 5 V point. The currents indicated at - 7 V and -12 V are then compared to the currents specified by the standard. The larger of the two voltage to current ratios forms the unit load value.

The electrical characteristics should not show any negative resistance otherwise instability and spurious oscillations could occur.

Total Load Characteristic Limits (RS-422)

In RS-422 the d.c load characteristics is specified much more simply;

The total load including multiple receivers, fail safe circuitry, and cable termination shall have a resistance greater than 90Ω between its input points (A and B), ie across the line, or when the cable is left un-terminated the resistance shall be greater than 400Ω, and shall not require a differential input voltage of more than 200mV for all receivers to assume the intended binary state.

With a basic understanding of transmission line practicalities, a brief discussion of the range of Texas Instruments products available and their application can begin.

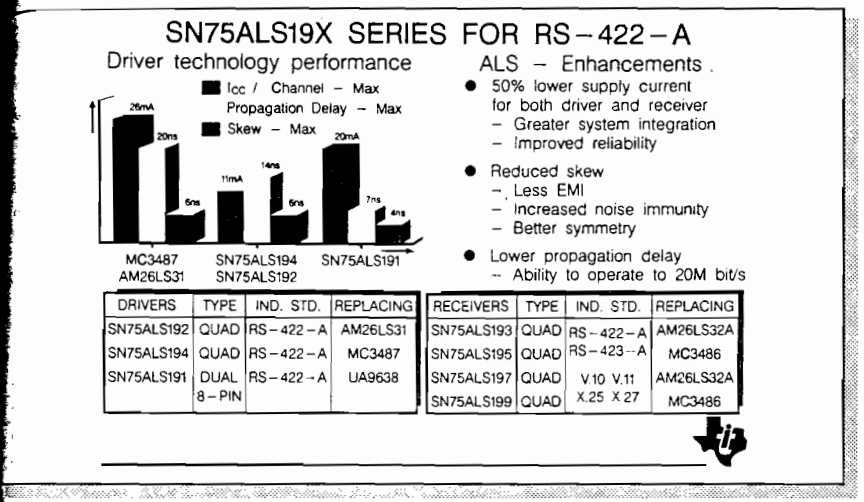


Figure 12 - SN75ALS19x Series For RS-422

The well proven SN75ALS19x series of drivers and receivers for RS-422-A represents some of the best speed versus power consumption alternatives in the industry today for reliable balanced line transmission over short as well as long distances. The series has found wide use in telecommunication as well as in computer applications.

ALS Technology Advantages

All ALS products employ Advanced Low-Power Schottky or Impact™ processes. These have been derived from the digital processes and trimmed for linear applications requiring wide common mode voltage operation, tough protection and accurate receiver input threshold

Notes

voltages. ALS technology provides combined improvements in die design, tooling produc
and wafer fabrication, which in turn, provide lower power consumption and permit much
higher data throughput than other designs - in short; speed without the usual power pena
Standby current is typically reduced by 50% although switching speed has gone up by mo
than 30% compared with previous LS (Low Power Schottky) parts.

50% Lower Supply Current

The significant reduction in power consumption allows for a higher board packaging den
and hence greater system integration without increasing temperature due to pow
dissipation. In addition, a lower operational temperature improves system reliability.

Lower power consumption also permits devices to operate in an extended temperature rang
(-55°C to +125°C) with fewer constraints.

30% Improvement in Data Throughput

Lower propagation delays and reduced skew, combined with lower standby power
consumption, allows these devices to operate in excess of 20Mbaud. For example; a
SN75ALS192 quad driver is capable of transmitting data at 20Mbaud (50% duty cycle) while
only dissipating the same power as an AM26LS31A in standby mode. The maximum
achievable data rate is usually determined by maximum power dissipation at the maximum
operating temperature. Reference should be made to the datasheet's Dissipation Rating
Table.

Impact is a trade mark of Texas Instruments

Reduced Skew

Skew for a data transmission driver or receiver is related to the difference in propagation
delays from input to output. With different high and low going propagation delays for a device,
asymmetry in its output signal occurs, which ultimately reduces the maximum data rate.

When switching the output of the differential driver from one state to the other state,
differences in propagation delays from the input to the inverting and non-inverting outputs can
cause the differential output voltage to flatten out as it passes through the receiver's threshold
region. Clearly, this makes the received signal more vulnerable to noise.

The SN75ALS19x series has been designed with minimum skew to improve symmetry,
increase noise immunity and radiate less EMI (Electromagnetic Interference) caused by
non-common mode currents in the transmission cable. The high-speed dual driver,
SN75ALS191 in an 8-pin package features a typical differential skew of 1.5ns (4ns
maximum).

Products

A wide range of SN75ALS19x products are available as improved pin for pin replacements for
industry standard devices.

main difference between the quadruple drivers, SN75ALS192 and SN75ALS194, is
ted to their enabling configuration. SN75ALS192 has a common pin enabling all four
ers, whereas independent enabling schemes are possible for each pair of drivers in the
75ALS194. Similarly, different enabling schemes distinguishes the quadruple receivers,
75ALS193 and ALS195. The SN75ALS192 and SN75ALS193 form complementary
ices as do the SN75ALS194 and SN75ALS195 devices. Using complementary drivers
receivers together should provide optimum performance.

e quadruple receivers, SN75ALS197 and ALS199 have relaxed input sensitivity
ecifications of ±300mV, compared to ±200mV for SN75ALS193 and ALS195. However,
y are available in low cost D (surface mount) or N (DIL) packages and meets CCITT
commendations V.10, V.11, X.26 and X.27.

Notes

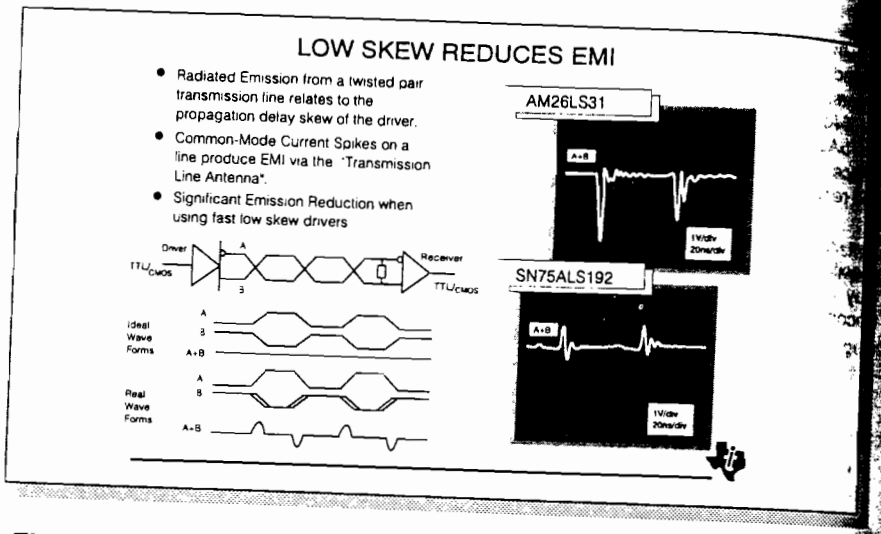


Figure 13 - Low Skew Reduces EMI

EMI Related to Differential Transmission Lines

Radiated emissions from electronic systems is having more attention paid to it, as mutual disturbances between electronic equipment increase and the subsequent need for EMC regulations becomes more apparant. This is compounded by the increased use of high clock rates and high currents which generate high frequency EMI. Applications placed on printed circuit boards are normally enclosed in a confined space making the problem easier to solve, but when transmitting data signals to the outside world through cables, increasing the total radiated emission by the system is difficult to avoid.

In large computer systems, Inter-unit cables within the system have been found to be responsible for much of the radiated emission. Further studies have revealed that the noise itself is a function of common mode current spikes, brought about by the skew between the outputs of clocked differential drivers. Significant improvements in system-wide emissions were seen in practice after replacing high skew driver devices with others those which had less skew.

The effect seen is not only related to large computer systems but is scaleable to all systems using differential transmission lines. Differential drivers and receiver are designed to operate under conditions with high common mode signals. Low frequency common mode signals usually cause no problems, but high frequency common mode spikes cause EMI and in systems with inter-unit cabling an antenna is readily available increasing the radiated emission. Clearly, twisted pair cables used to interconnect boards within the same cabinet, or

establish data transmission between various equipment, using for example the popular standards RS-422-A or RS-485, are likely to radiate EMI if the driver's complementary outputs are not exactly symmetrical. This is true for the single differential line in an industrial system as well as for the many parallel differential lines used in a SCSI interface cable.

Low Skew Devices Reduce EMI

Ideally, a differential driver should not generate common mode signals due to the nature of the differential output and the twisted cable cancelling the common-mode currents but in practice, small differences between the complementary outputs occur which produce fast common mode pulses on the line.

The skew specification, specified as the propagation delay difference from the input of the differential driver to the driver's respective inverting and non-inverting outputs is a good measure for how much or how little radiation that can be expected from high frequency common mode signals during switching. However, a low skew specification on its own does not guarantee negligible common mode signals as the signals can still be unsymmetrical due to different rising and falling waveforms. In such cases Significant current spikes can be measured on the line.

Use Fast Devices Even in Low Data Rate System

Even in systems where low data rates are used, EMI can still cause problems with EMC regulations. These problems are best solved by employing high speed devices usually having a significant lower skew than slower drivers.

Consequently, previous low power schottky (LS) designs like, AM26LS31 or SN75176 will in general radiate more emissions than newer Advanced Low Power designs like SN75ALS192 and SN75ALS176 or even the new BiCMOS designs like AM26C31 and SN75LBC176. A measurement was made to demonstrate this effect comparing AM26LS31 with SN75ALS192. Evidently, the negligible common mode signals resulting from switching the SN75ALS192 are significantly smaller than the clearly visible common mode current spikes produced by the AM26LS31.

Notes

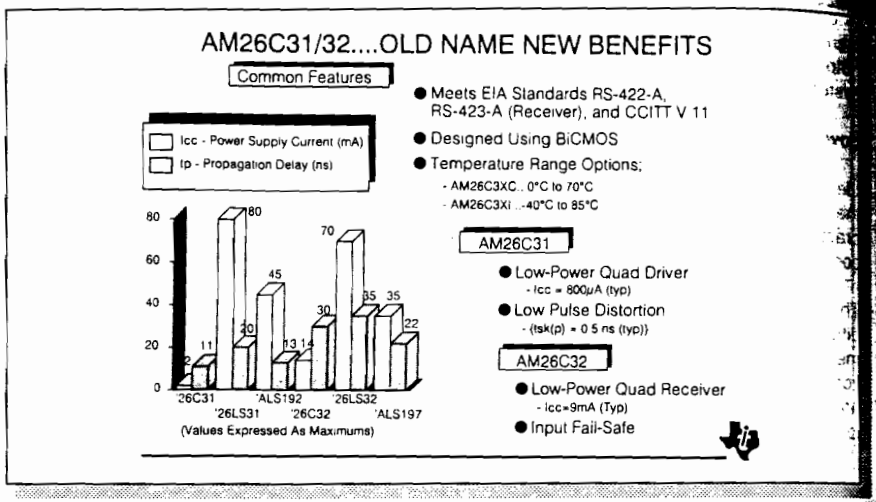


Figure 14 - AM26C31/32....Old Name New Benefits

Improvements in Power Consumption and Speed

Industry has long been aware of the advantages gained from using the quadruple driver AM26LS31 and the accompanying quadruple receiver AM26LS32 for RS-422 type applications . However the old low power schottkey (LS) process is no longer capable of keeping pace with todays demands for high speed and low power. The AM26C31 and AM26C32 are modern upgrades, fabricated using a low power BiCMOS process.

These devices find applications where high speed and low skew are crucial, for example in disk drive and Telecommunication applications. One particular application which would benefit from the low power consumption will be the Central Office Exchange, where due to the shear number of devices used, power consumption becomes a critical issue - especially when the rest of the system is implemented in low power CMOS.

The figure shows some key benefits of these new designs and compares the power consumption and propagation delay against industry standard devices. It can easily be seen that the BiCMOS devices not only exhibit a dramatic reduction in power consumption, from 80 mA to 2 mA, but there is also an improvement in ac performance. The AM26C31 driver has a lower propagation delay than any of the devices shown in the graph.

Description

Both the AM26C31 and AM26C32 have been manufactured using a BiCMOS technology which is a combination of bipolar and CMOS transistors. This process provides the high

oltage/current drive of bipolar with the low quiescent power consumption of CMOS. The raphs in the figure show that the power consumption of the AM26C32 receiver is reduced to pproximately one-fith of the standard LS part.

he AM26C31 is a quadruple complementary-output line driver designed to satisfy the equirements of EIA RS-422-A and CCITT recommendation V.11. The three-state outputs ave a high-current drive capability for driving balanced lines such as twisted-pair or parallel-ire transmission lines, and they provide a high impedance state in the power-off condition. he enable function is common to all four drivers and offers the choice of active-high or ctive-low enable input.

he AM26C32 is a quadruple line receiver for balanced and unbalanced digital data ransmission. Conformance to the EIA standards RS-422-A and RS-423-A and CCITT ecommendation V.11 is guaranteed. The enable function is common to all receivers and ffers a choice of either active-high or active-low inputs. Three-state outputs permit onnection to a digital data bus. Fail safe circuitry design on the receiver input side ensures hat the outputs will remain in a high state even if the inputs are left open. This reduces the hances of incorrect data interpretation.

Notes

Protecting Against Data Corruption

One noted feature offered by the AM26C32 receiver was an built-in fail safe feature. This feature is also a requirement in many RS-485 applications, however its usefulness need be considered and understood at an application level.

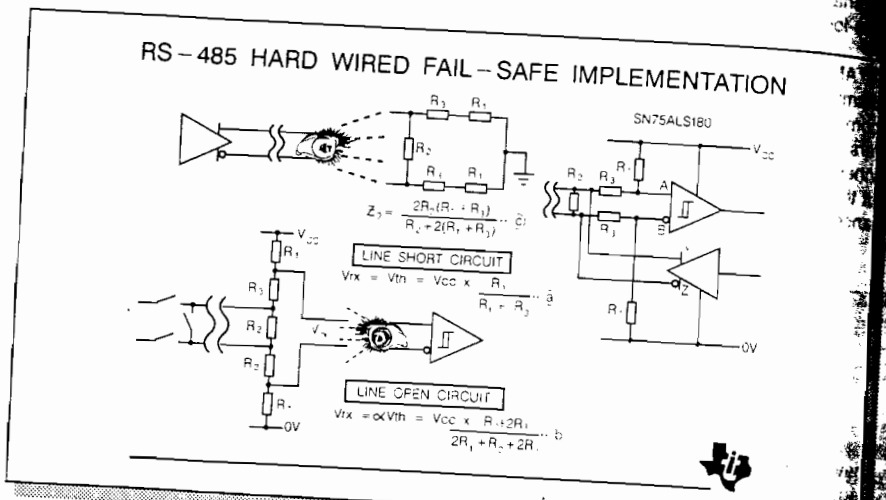


Figure 15 - RS-485 Hard Wired Fail safe

The need For Fail safe Protection

In any party line interface system, with multiple driver/receivers, there will be long periods of time when the driving devices are in-active. This state known as line idle occurs when the drivers place their outputs into a high impedance state. During line idle, the voltage along the line is left floating, i.e. indeterminate - neither logic high or logic low. As a result the receiver could be falsely triggered into either a logic high or a low logic state, depending upon the presence of noise and the polarity of the floating lines. This is obviously undesirable as the circuitry following the receiver could interpret this as valid information. The receiver should be able to detect such a situation and place its outputs into a known, and pre-determined state. The name given to methods which ensure this condition is called **fail safe.** An Additional feature which a fail safe should provide is to protect the receiver from shorted line conditions which can again cause erroneous processing of data and/or receiver damage.

ere are several ways implement a fail safe, including a hard-wired fail safe using line bias istors or protocols. Protocols, although complicated to implement, are the preferred thod and are discussed in more detail following this section. However since most system signers. hardware designers in this case, prefer to implement such functions in hardware hard-wired fail safe is often implemented.

hard wired fail safe should provide a defined voltage across the receiver's input whether or t the line is shorted to either supply rail or is left open circuited. The fail safe should also be corporated into the line termination network when at the extremes of the line.

ternal Fail safe

Manufacturers have gone part way to facilitating fail safe design by including some form of pen line fail safe circuitry within the integrated circuits. Unfortunately, due to power consumption constraints, the extra circuitry has proved little use. The extra circuitry is quite ften just a large pull-up resistor on the non-inverting receiver input, and a large pull-down esistor on the inverting input of the receiver. These resistors are normally in the range of 100kΩ. and so when used in conjunction with line termination resistors to form a potential divider, only a few milli volts are generated. As a result this voltage (receiver threshold voltage) is insufficient to switch the receiver. In effect, to use these internal resistors no line termination resistors can be used, which reduces the allowed reliable data rate enormously.

External Fail safe-Open Line Conditions

A more reliable way of offering open line fail safe is to use external pull-up and pull-down resistors. There two basic ways of doing this; one way is to polarise the line with the pull-up/pull-down resistors and use these resistors to match the line impedance. Another way is to use larger polarising resistors while using an extra resistor to terminate the line. The first idea has one advantage in that it provides a low impedance path to an a.c. ground, so that any currents induced on to the line have a low impedance path to ground. However a problem is encountered with this method because the driver output now has to drive very much lower impedances. If the driver output current capability is poor the device could easily go into output short circuit current limit. The second way, although requiring an extra resistor will not load the driver's output to such an excess.

Notes

Placing external pull-up and pull-down resistors R_1 on the non-inverting and inverting inputs of the receiver will produce open circuit fail safe. Terminating the transmission line with its characteristic impedance.Z_O , produces a potential divider between $2R_1$ and Z_O. The voltage formed across the line, V_{OC}, equals

$$V_{OC} = V_{CC} * \frac{Z_O}{2R_1 + Z_O}$$

Devices meeting the RS-485 receiver threshold voltage specifications require V_{OC} to be greater than 200mV . From this the relationship of R_1 to Z_O can be derived:-

$$R_1 = Z_O * \frac{1}{2} * \frac{V_{CC} - V_{OC}}{V_{OC}}$$

With V_{CC} = 5V, V_{OC} = 200mV and Z_O = 100Ω, yields R_1 = 1.2kΩ.
Biassing the receiver in this way will only provide open line fail safe, it will not provide shorted line fail safe. However, when using transceivers it is not possible to provide shorted line fail safe configurations, this ia result of the driver and receiver sharing the same i.c. pins. Hence for devices like the SN75ALS176 this open line configuration the optimum fail safe available.

External Fail safe-Shorted Line Conditions

To implement protection from the shorted line condition, further resistors are required. When the line is shorted the transmission line's impedance goes to zero and the termination resistors will also be shorted. Putting extra resistors in series with the input to the receiver can provide shorted line fail safe protection.

The extra resistors, R_3 in the figure, can only be added when using devices with separate driver outputs and receiver inputs. So internally wired transceivers cannot be used to offer shorted line fail safe. If this form of protection is required then a device such as the SN75ALS180, with its separate driver outputs and receiver inputs, should be used. If a transceiver type device was used then the extra resistors R_3 would cause extra attenuation of the output signal. The ALS180 will have its driver outputs fed directly to the line, bypassing resistors R_3.

Calculating the Resistor Values

If the line became shorted then R_2 would be removed leaving a voltage across the receiver inputs of:-

$$V_{rx} = V_{CC} \times R_3/(R_1 + R_3) \qquad \textbf{(a).}$$

For RS-485 and 422A applications the standard specifies V_{rx} to be greater than 200mV. So $V_{rx} = V_{th}$ = 200mV. Using this figure, along with the minimum permissible supply voltage for the devices gives a relationship between R_1 and R_3.

When the line goes into a high impedance state the receiver will see the two R_3 in series with R_2 plus the two R_1's pulling up and down on either input. The receiver input voltage will now be:

$$V_{rx} = V_{CC} \times (R_2 + 2R_3)/(2R_1 + R_2 + 2R_3) \qquad \textbf{(b).}$$

Relating this new V_{rx} to the minimum specified in the standard, V_{th}, gives:

$$R_1 = ½R_2 \times \left[\{(V_{CC} - \alpha V_{th})(V_{CC} - V_{th})\}/\{(\alpha - 1)\, V_{th}\, V_{CC}\}\right]$$

$$R_3 = R_2 \times (V_{CC} - V_{th})/V_{th}$$

The transmission line will see an effective line termination resistance of R_2 in parallel with twice the sum of R_1 and R_3. This should match the transmission line's characteristic impedance, Z_O, therefore

$$Z_O = 2R_2 \times \frac{R_1 + R_3}{2R_1 + R_2 + 2R_3} \quad \textbf{(c)}$$

Combining equations **(a)**, **(b)** and **(c)** yields the following equations for R_1, R_2 and R_3:-

$$R_1 = ½Z_O \times \frac{(V_{CC} - V_{th})^2}{(\alpha - 1)\, V_{th}\, V_{CC}}$$

$$R_2 = Z_O \times \frac{V_{CC} - V_{th}}{V_{CC} - \alpha V_{th}}$$

$$R_3 = ½Z_O \times \frac{V_{CC} - V_{th}}{\alpha - 1\ V_{th}}$$

Notes

In this application assuming the supply voltage is 4.5V and Vth = 200mV with an a value of 1.5 and driving a line with characteristic impedance of 120Ω yields the following values:-

R_1 = 2.2kΩ
R_2 = 120Ω
R_3 = 110Ω

The values of R_1, R_2, and R_3 only apply for receivers at the extreme of the line; if there are more receivers on the line then fail safe can be accomplished by multiplying the values of R_1 and R_3 by half of the number of receivers on the line. This is done by assuming the input stages of all the receivers are the same, all R_1 resistors are the same, and that all R_3 resistors are the same. Since all of R_1 and all of R_3 resistors will be in parallel, their overall resistance will be divided by half the number of receivers. If there is a large number of receivers on the line there is a danger of R_3 becoming too large and forming a large potential divider with the input resistance of the receiver, normally around 18kΩ.

Use of Protocols- Synchronous Serial Communication

The use of line terminations to effect a fail safe is not a recommended practice. The recommended practice is to use software protocols. Protocols come in many forms (two of which are explained below) and provide a set of rules which define the meaning and order in which data should be sent. In particular, they can be used to provide a fail safe feature and be used to avoid contention. Contention occurs when several drivers try to address the link at the same time. This can lead to high current sinking or souring leading to excessive thermal dissipation in the drivers. Fail safe is ensured by allowing the receiving station to respond to valid data only., This is achieved by sending a preamble before each data packet . The preamble consists of a pre-determined pattern of bits, which signals to the receiver that valid data is about to follow. Anything other than this preamble should be ignored by the receiver.

Party Line Protocol Formats

Party line applications use either half duplex or full duplex transmission. Half duplex's transmission mode is where two terminals (a driver and receiver) can communicate with each other bidirectionally over the same link, but they cannot transmit simultaneously. A party line transmission line format can be achieved using half duplex by multiplexing between a number of driver/receiver pairs. Full duplex communications involves the simultaneous, two way flow of data from driver/ receiver pairs.

A communication line uesd in a multiplexed operation such as the half duplex party line system reduces wiring costs when compared to the simplex operation (simplex one driver for one receiver). Only one line is needed to implement the communication system, though control of the multiplexing does require complex protocol or handshaking circuits.

A typical (simplified) protocol sequence would contain the following elements;

i) **Driver requests access to communication link (bus)**
ii) **Link controller responds to request and gives go ahead when bus is free**
iii) **Driver gains bus mastership and sends data which is preceded by a destination code**
iv) **Receiver sends an acknowledgement**
v) **Driver receives confirmation and releases the bus**

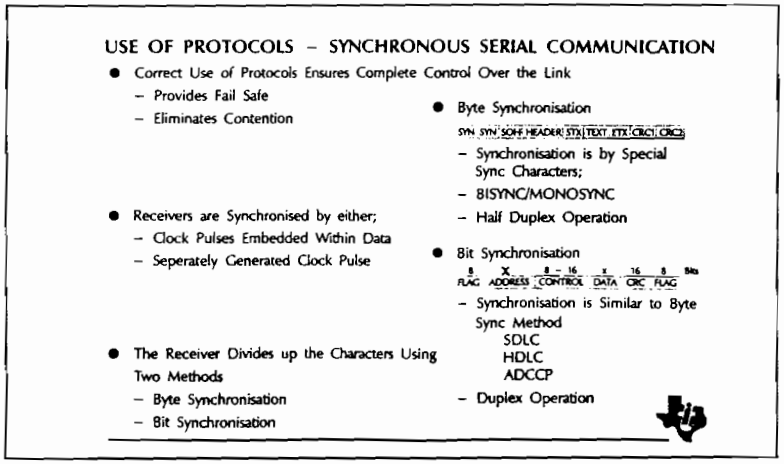


Figure 15a - Use of Protocols in Synchronous Serial Communications

Synchronization

Some form of synchronization is necessary for the receiver to determine the start and finish of the received bits. Two schemes, with many variations, are adopted; *Asynchronous* and *synchronous.*

Notes

Asynchronisation, or start-stop bit communication, uses a system where characters are sent one at a time, without necessarily having any fixed time relationship between each other. In such a case the driver sends start bits followed by the information field, followed by one or more stop bits. This informs the receiver that information data will follow the start bit and will end prior to the stop bit. The data is usually broken into small groups of 8-bits, one byte, which is preceeded with a start bit and concluded with a stop bit. This is one of the schemes employed by RS-232.

Synchronous transmission is used to transmit complete blocks of data at one time.In synchronous transmission the duration of each bit is the same. With all characters being the same length the receiver only has to identify the first character and then clock the others in at a predetermine rate.

Serial synchronous communication uses a similar scheme and either embeds the timing information in the data or provides a separate clock signal. However the bit stream still has to be divided up into the individual characters. There are two main methods of achieving character synchronization: *Byte synchronization and bit synchronization.*

Byte synchronization, one of the first synchronous methods to be introduced is best known by IBM's bisync and monosync . Synchronization is achieved by using special *SYNC* characters which are transmitted in between data packets. The receiver continually monitors this transmission and uses it to synchronize itself . After receiving one (monosync) or two (bisync) sync pulses the receiver is said two be in the synchronized mode and is ready to receive data. Synchronization is ensured by re-sending the sync bits every few hundred characters, for this reason data is grouped together in frames or packets which start with sync characters. Each frame is 8-bits long

The bisync protocol also defines a structure for a frame that includes control information and error checking capability. The figure shows the basic frame structure with the sync characters followed by the header field. *SOH* identifies the beginning of the header block. The *header* field is user defined and generally contains control specific information such as rest data link, message numbering priority ..etc. Start of text, STX, identifies the end of the header field and defines the beginning of the text field. The text or data field contains application specific information which must be sent to the application controller intact. ETX signals, end of text, and CRC1 and CRC2 are used as cyclic redundancy check bits. Notice that STX, ETX etc.. are the standard ASCII control codes. Bysync is essentially a half duplex system because each frame requires an acknowledge from the receiver before commencing with the next frame. Obviously sending acknowledging codes back and forth reduces the data rate, and to overcome this bit synchronization was developed.

SDLC (synchronous data link control), again made popular through IBM, was one of the first bit synchronization protocols available. The CCITT also adapted this standard for their high level data link (HDLC) protocol. Both are very similar to the CCITT X25 layer 2 packet switching local area networking standard. Initially bit sync looks very similar to byte sync , ie during data null periods sync pulses are sent over the link to synchronise the receiver and driver. However after the sync period the data may be grouped in any number of bits. Byte-sync systems are restricted to 8-bit packets. In SDLC and HDLC, messages are formatted into frames with each frame being divided into fields. The start flag is the sync data while the

address field contains the destination address to select the required receivers. The control field can be configured as either an information field or supervisory field. The information field, which is the usual format, contains status information on the number of frames sent or received. Data field follows and contains application specific code. The supervisory or management frame is used to acknowledge successful receipt of data. CRC is used for error checking and flag is the next sync signal.

Party Line Considerations

The following points should be considered for correct party line operation;

i) Each driver must have a three-state logic capability, two logic states and a high impedance mode. Also at any one instance it is likely that all drivers could be in the high impedance state, thus leaving the bus floating. A receiver should be able to detect this situation and protect against any spurious information - fail safe design.

ii) Receivers may oscillate if left unconnected, which might affect other used receivers in the same package. Therefore it is recommended that all unused receiver inputs should be tied to defined logic states.

Notes

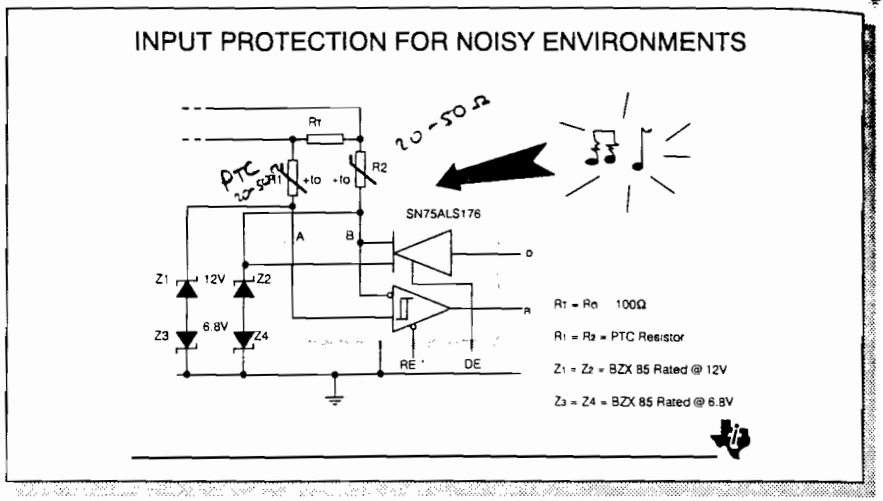


Figure 16 - Input Protection In Noisy Environments

In addition to fail safe protection, applications often require protection against excessive noise voltages.

Often when sending data over long distances or in electrically hostile environments, i.e. factory automation, the noise immunity afforded by the differential transmission scheme, and in particular the wide common mode voltage range of RS-485 is insufficient. This figure shows how external diodes offer transient spike protection for the SN75ALS176 RS-485 transceiver.

R_T is the usual termination resistance and is equivalent in value to the characteristic impedance of the line. Positive Temperature Coefficient resistors, R_1 and R_2, provide current limiters for the diode chain. Provided their ambient temperature resistance is kept below 50Ω they will be transparent during normal usage and will not alter the termination value or attenuate the driver output voltage.

Z_1 and Z_2 are chosen to protect the input from positive spikes greater than 12 V whilst Z_3 and Z_4 protect the device from negative going spikes greater than -6.8 V.

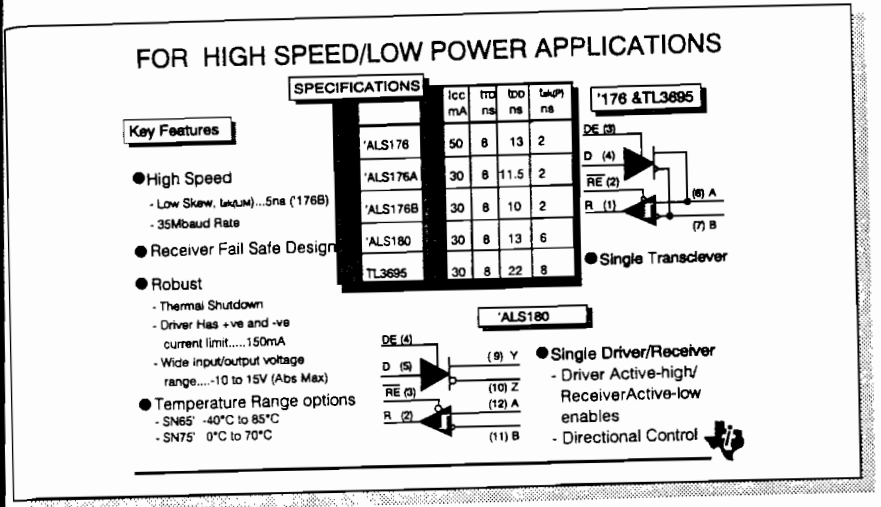


Figure 17 - SN75ALS' Series for High Speed/Low Power Applications

Product Description

In the previous noise protection example, the SN75ALS176 was introduced. This device forms just part of a range of high performance single line driver/receiver options available for RS-422 and RS-485 applications. Some key benefits of this range are discussed in the following text.

The range of devices shown in the figure are all high speed low power monolithic integrated circuits, designed for bidirectional data communication on multipoint bus transmission lines. The SN65ALS176, SN75ALS176 series and TL3695 are single differential transceivers, while the SN65ALS180 and SN75ALS180 are a single differential driver/receiver pair.

All devices are designed for balanced transmission lines and meet EIA standards RS-422-A and RS-485, CCITT recommendations V.11 and X.27, and ISO 8482:1987(E).

Notes

The SN65ALS176, SN75ALS176 series and TL3695 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver's differential outputs and the receiver's differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimal loading to the bus whenever the driver is disabled, or V_{CC} = 0V. This port features a wide positive and negative common-mode voltage range making the device ideal for party line applications. All devices are available in either 8-pin dual-in-line plastic (P) or 8-pin plastic small outline surface mount (D) packaging.

The SN75ALS180 contains many of the same features listed above. However, the driver outputs and receiver inputs are not internally connected together but are brought outside the chip, offering a separate driver and receiver function. For this reason the SN65ALS180 and SN75ALS180 are housed in a 14-pin dual-in-line plastic and 14-pin small outline plastic packages. This arrangement makes the SN75ALS180 ideal for full duplex operation.

Product Differentiation

The SN75ALS176 series allows the designer to select between ac performance levels. The figure shows the maximum propagation delays and skew specification for the range. The SN75ALS176B offers the highest speed performance with a maximum differential output delay time of 10ns. With a minimum specified value of 5ns the device is capable of data rates in excess of 60 Mbaud (as per RS-485 specification).

Perhaps even more importantly, especially for high speed multi-channel applications (for example SCSI), is the low skew value, $t_{sk(LIM)}$. In this instance skew is specified as the difference between the maximum and minimum differential output delay times, T_{DD}. The SN75ALS176B has a minimum $t_{sk(LIM)}$ value of 5ns. This value is used to determine the delays in signals between channels in the system. The pulse skew, $t_{sk(P)}$, is specified as a minimum value of 2ns (See 'A discussion of Skew' in the 'The specifications and Transmission line practicalities 'section for further information).

The TL3695 provides the same functionality as the 'ALS76 series of devices, but is aimed at lower performance lower cost systems.

As the application areas for multi-point differential standards standard widen so to do the applications for the transceiver function.

On such emerging application is in the industrial environment, to connect between control modules (Masters) or process sensors (slaves). For this reason Texas Instruments has included the '65' temperature range option which extends the temperature range from the basic 0°C to 70°C option to -40°C to 85°C.

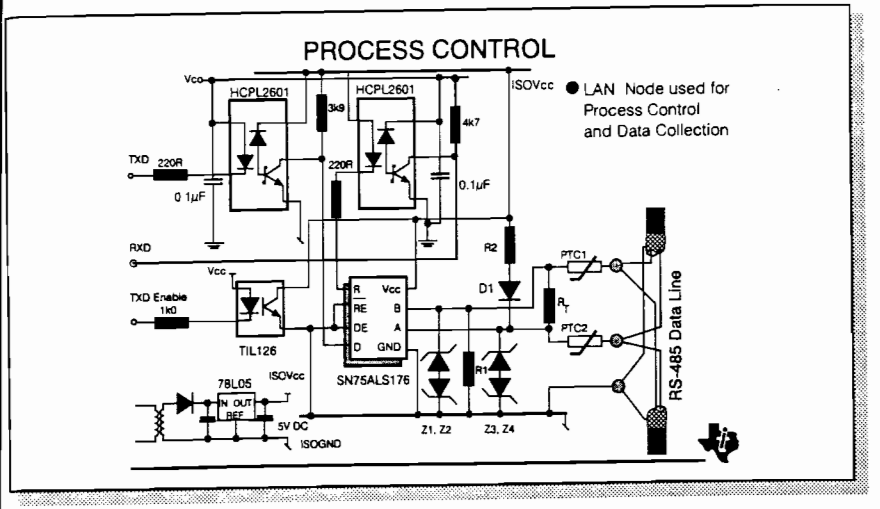


Figure 18 - Process Control Application

Process Control

In the previous sections the need for line termination, receiver fail safe and noise protection was highlighted. All these elements can be found in an industrial process control and data collection application, which is shown in the figure.

The need For Galvanic Isolation

The capability of meeting toughened noise legislation is a key requirement for many new end products and applications. Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer, and a proven route to improved noise performance for any interface system is galvanic isolation.

Notes

Such isolation in data communication systems is achieved without direct galvanic connection or wires between drivers and receivers. Magnetic linkage from transformers provide the power for the system, and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines and hence the impressed noise voltages which affect the signal are also eliminated. Common mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique.

Taking a more practical view of where problems are likely to occur when using a galvanic interface, can be found in the industrial environment. For example consider the case when the interface node, shown in the figure, connects between a data logger and a host computer via the RS-485 link. When an adjacent electric motor is started up, a momentary difference in ground potentials at the data logger and the computer may occur due to a surge in current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and in the worst case damage to the computer could occur.

Circuit Description

The schematic shown forms an interface, one node, for a "distributed controlling, regulation and supervision (DCRS) system". Such a scheme could be used in a 'Field bus' type application. Transmission takes place via a 2-wire bus, formed by a twisted-pair, shielded cable connected in a ring circuit. Other nodes, master or slaves, may be distributed along the bus in an arbitrary fashion and may be separated hundreds of metres in distance.

The bus driver used is the **SN65ALS176**, chosen for its high data rate capability and low power consumption. Low power is crucial in this type of application since many remote outstations will either be battery operated or require battery back-up capability. The '65' option was chosen for its industrial temperature range of -40°C to 85°C.

Transceiver protection circuitry is formed by Z_1,Z_2,Z_3 and Z_4 along with current limiters PTC_1 and PTC_2 (see previous example). Line termination is formed by a combination of R_T, R_1 and R_2. The values of which can be calculated as follows;

$$R_1 = R_2 < 0.5 \times Z_O \times [1 + V_{CC}/V_{TH}]$$

and

$$R_T = Z_O [1 + V_{TH}/V_{CC}]$$

Using a cable with a characteristic impedance of $Z_O = 120\Omega$ and a desired V_{TH} of 200mV, requires $R_1 = R_2$ to be around $1.6k\Omega$ in value. The terminating resistor, R_T would be in the order of 124Ω.

The inclusion of $R_1 = R_2$, provides a receiver fail safe to open line conditions by biasing the polarity of the line to a logic '1' under line idle conditions.The values of $R_1 = R_2$ are best kept as low as possible to increase the noise rejection when the line is left floating, but they will place some loading onto the driver.

Galvanic isolation is afforded by means of three optocouplers/optoisolators. The HCPL2601 is chosen for its high data rate capability, t_p = 75ns (max), and its high voltage isolation.

The HCPL2601 is designed for use in high speed digital interfacing applications that require high voltage isolation between the input and output. Its use is highly recommended in extremely high ground noise and induced noise environments.

The HCPL2601 consists of a GaAsP light emitting diode and integrated light detector, composed of a photodiode, a high gain amplifier and a Schottky clamped open collector output transistor. An input diode forward current of 5mA will switch the output transistor low, providing an on state drive current of 13mA (eight 1.6mA TTL loads). A TTL input is provided for applications that require output transistor gating.

Housed in a single 8-pin dual-in-line plastic package the HCPL2601 is characterised for operation over the temperature range of 0°C to 70°C. The internal Faraday shield provides a guaranteed common mode transient immunity of 1000V/µs.

A 0.1µF capacitor has been connected between V_{CC} and ground to improve switching performance.

Automotive Applications

Other emerging application areas are in the automotive industry, where even higher demands are made on the temperature range options of line interface circuits. One such area is the use of data transmission devices in low power data distribution systems, known as multiplex wiring.

Although the gradual trend in automotive applications is towards full multiplex wiring, where one common bus runs throughout the car (described below), an interim solution is to use several buses serving common systems.

Notes

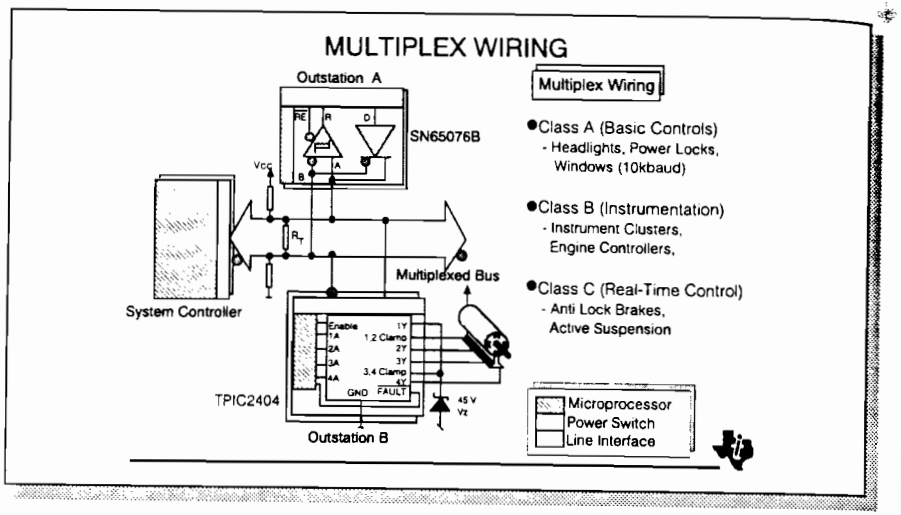


Figure 19 - Multiplex Wiring

Multiplex wiring is seen as a way to replace the costly and cumbersome conventional wiring harness that runs throughout the car. This harness, made up of thick copper wire and heavy duty switches is used to deliver the full load current from the battery to the load (actuator, lamp..etc) This approach as well as being costly is heavy, very difficult to test for faults, repair and is inflexible. Although the use of multiplexing is ultimately seen as giving cost advantages its more immediate use is to fix the afore mentioned problems.

In a typical multiplexed system, a central controller will communicate with 'outstations' (which house both the control switches and load drivers) via a common distributed bus. Typical components of the system, shown in the figure, will require a system controller, differential line driver/receiver and intelligent power switch.

The central controller is responsible for implementing the communications protocol, which allows data, status, address and control information to be exchanged with the outstations. Part of the information exchange could be diagnostic data from the outstation power switch, used for driver instrument panel information or fault diagnosis during repair.

The central controller communicates over the bus via line interface devices. Due to the electrical hostile environment and the need for high reliability (especially in safety critical applications) a differential data transmission scheme is used which gives increased noise immunity.

The final requirement is for a local intelligent power device, which exchanges the low voltage TTL/CMOS logic level from the interface device to a high current, high voltage level to control the actuator. In addition to their power transfer characteristics, these devices should provide

simple error sensing capabilities which can detect device or actuator problems. Such a device could be the **TPIC2404** which is a monolithic high-voltage high-current quadruple low-side switch.

Automotive data buses can be broken down into three main categories;

Class A buses include basic controls, such as headlights, power locks and widows;

Class B buses cover instrument clusters, engine controllers, trip computers and other areas requiring exchange of information;

Class C buses, which are the furthest from implementation, include real-time control applications, for example anti-lock brakes, active suspension systems, and other engine controls.

The application and position of the outstation dictates the temperature range required from the interface circuit. For example outstations situated in the engine compartment will require a wider operating range than an outstation situated behind the instrument cluster.

Product Support

Texas Instruments has an on-going programme to provide interface devices which support all the major automotive standards. These standards include the SAE J1850 standard and European standards CAN and VAN. Of particular note are the LinBiCMOS developments for the J1850 standard. These devices are differential current mode line/drive receive devices which contain over 300 logic gates for memory buffering, thus allowing message handling capability. Use of LinBiCMOS provides the robustness, wide voltage ranges and extended temperature ranges required for automotive applications.

Early implementors of partial multiplex wiring systems have capitalised upon the advantages offered by the SN65176B device. However for real high temperature application, (i.e. outstation situated in the engine compartment) further temperature range extensions are required. For this reason the **SN65076B** was developed, and is characterised for operation from -40°C to 105°C. Special selections may extended this range further still.

The SN75076B achieves this high temperature range of operation by application optimisation, i.e. by eliminating all unnecessary functions the device's power dissipation can be kept to a minimum. For example, complicated enabling schemes are not required since most

Notes

automotive electronic designers using the SN75176B hardwire the driver input either high or low and apply the signal input to the enable. This provides one active state (driver enabled) and one passive state (driver disabled). To enable this to function correctly a three resistor termination network is required, such that resistors polarise the line to the opposite polarity as the driver leaves its active state. Therefore the driver input circuitry and one half of each input are redundant. The SN75076B removes this circuitry, thus reducing its device power dissipation. Additionally the cable lengths are quite short so there is no need for a high current drive capability Hence the SN75076B has an output current drive capability of only ±10mA, which while reducing the power dissipation overheads further, is still more than adequate for multiplex wiring applications.

Product Description

The SN65076B and SN75076B differential bus transceivers are monolithic integrated circuits, designed for bidirectional data communication on multipoint bus transmission lines. They have been optimised for use in noisy environments, for example automotive, where a low impedance termination to ground is required.

The SN65076B and SN75076B combine a differential line driver and a differential line input receiver, both of which operate from a single 5V power supply. The receiver has an active-low enable. The driver's differential outputs and the receiver's differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimal loading to the bus whenever the driver is disabled, or V_{CC} = 0V. This port features a wide positive and negative common-mode voltage ranges making the device ideal for party line applications.

The driver is designed to handle loads up to 10mA of sink (B I/O) and source (A I/O) current. The driver features positive and negative current limiting and thermal shut-down for protection from line fault conditions. Thermal shut-down is designed to occur at a junction temperature of approximately 150°C in the P package and 170°C in the D package. The receiver features a minimum input impedance of 12kΩ, an input sensitivity of ±200mV, and a typical hysteresis of 50mV.

Both devices are available in either 8-pin dual-in-line plastic (P) or 8-pin plastic small outline surface mount (D) packaging. The SN65076 is characterised for operation from -40°C to 105°C and the SN75076 is characterised for operation from 0°C to 70°C.

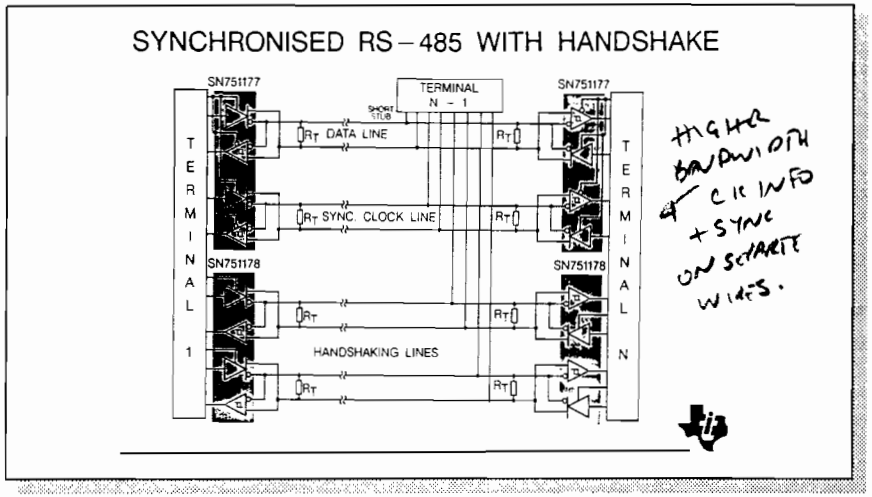


Figure 20 - Synchronised RS-485 with handshake

Boost the Data Rate

Most RS-485 systems operate with a single twisted pair as the data transmission medium limiting the data transfer to asynchronous mode. In addition, the single line must also transfer receiver address, start and stop bits and a preamble to enable the receiver logic to distinguish between data or rubbish on an idle line. These additional transferred bits impact the speed of operation on the data line.

Alternatively, synchronised data transfer can be implemented by adding an additional sync. clock line as shown on the figure, and can be further complemented with the addition of a couple of handshake lines. The overall transfer of the "real data" can be significantly speeded up, as most of the control bits used in asynchronous mode will be eliminated from the data path.

Notes

Specifically, synchronous data transfer benefits from applications where complete blocks of data can be transferred because the usual requirement in asynchronous transfer for breaking the data down in small groups of 8-bits (proceeded with a start bit and concluded with a stop bit) is eliminated.

Several terminals or station can be connected to this synchronised RS-485 system. The number of stations is only limited by the usual rules for RS-485. Daisy-chain connection between terminals is required unless each terminal is connected to the main data path via a short stub as the shownfor terminal number N - 1.

Why use the SN751177 and SN751178 ?

The SN751177 contains two drivers and two receivers in a single 16-pin package. Each pair of drivers and receivers has a common enable line. Upon transmission, both the data and sync. clock drivers are enabled allowing synchronous transfer of data. When shifting to receiver mode, both drivers are disabled, and the two receivers are enabled simultaneously. Due to the complementary enabling schemes for drivers and receivers (logic 1 enables the drivers but disables the receivers, and logic 0 the opposite), it is possible to connect both driver and receiver enable signals to the same control output. This reduces the number of I/O's required.

The SN751178 also contains two drivers and two receivers in a 16-pin package, but offers a different enabling pattern. The two receivers are always active and listen continuously to the handshake lines as necessary. However, the two drivers can be independently enabled as required by a handshaking scheme.

In summary, the SN751177 and SN1178 offer a simple but versatile solution sunchronous transfer of data at high speeds. Their configuration as two driver/receiver pairs adds to the effectiveness of the application

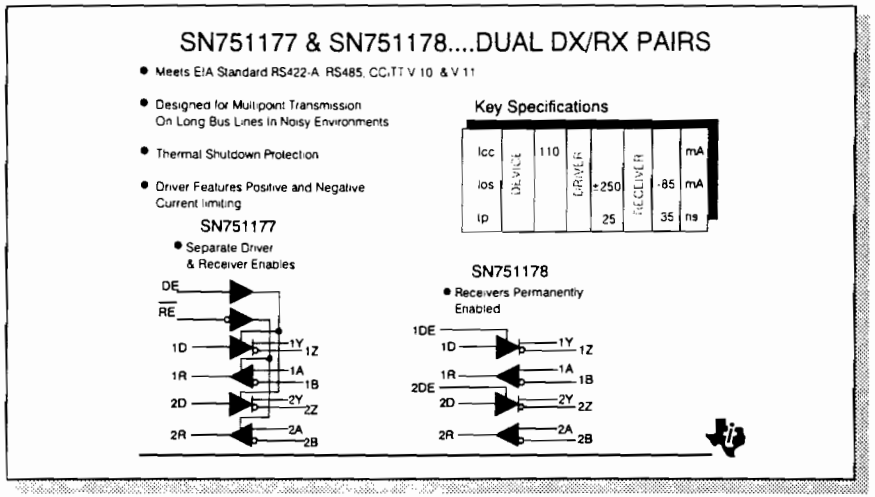


Figure 21 - SN751177 and SN751178 Dual DX/RX Pairs

Product Description

The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits designed for balanced multipoint bus transmission at data rates up to 10Mbaud. They are designed to improve the performance of full-duplex data communications over long bus lines and meet EIA standards RS-422, RS-485 and several CCITT recommendations.

The SN75117 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on the transmission line.

The receiver features include a high input impedance of 12kΩ, an input sensitivity of ±200mV over a common-mode input voltage range of -12 V to +12V and a typical hysteresis of 50 mV. A fail safe feature ensures that if the receiver inputs are open, line idle, the receiver outputs will always be high.

Notes

The SN751177 drivers and receivers are enabled in pairs. An active-low RE enables both receivers, whilst an active-high DE enables both drivers. The SN751178 has an enable for each driver, whilst its receivers are permanently enabled. Choice of enabling scheme offers flexibility in application, allowing use as repeaters, direction control or data lines in full, half duplex and simplex modes of operation.

Both the SN751177 and SN751178 are characterised for operation from -20°C to 85°C, and are available in 16-pin dual-in-line plastic packages.

Future developments of these products will include ALS-Impact™ versions resulting in lower power consumption and increased speed.

Impact is a trade mark of Texas Instruments

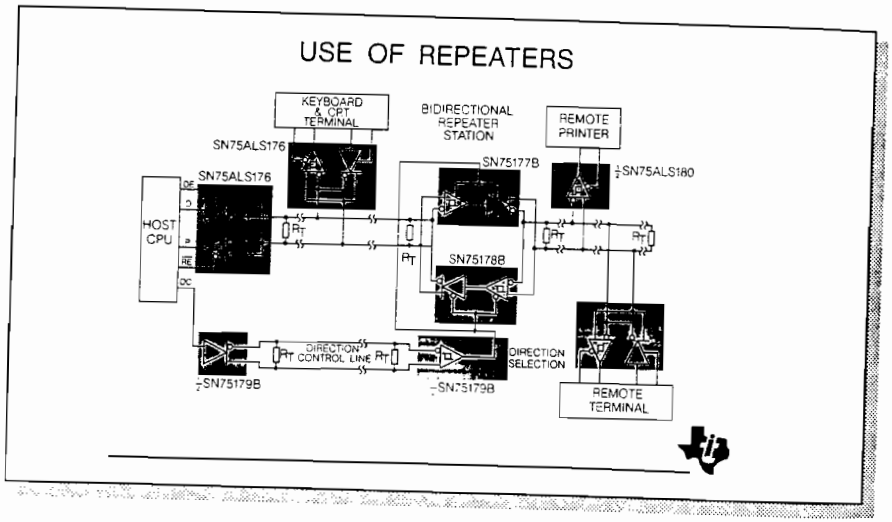


Figure 22 - Use of Repeaters

The Need for Repeaters

The major advantage of RS-485 is that it permits multiple drivers and receivers to operate over a 2-wire bus, thus setting up a party-line architecture. When such a data communication bus system is transmitting data over lines as long hundreds of meters or even thousands of metres, attenuation is often experienced between a driver at one end and a receiver in the other end (over long distances the cable's resistance does have an effect). Such systems can benefit from the use of signal restoration by means of bus repeaters.

Similarly, when more than 32 unit loads are connected to a bus, requirements for additional buffering arise. A bus repeater has in this function a different role from restoring the original signal namely to drive another 32 unit loads.

Repeater Solutions

Bus repeaters in data communication systems receives degraded signals from the transmission line, squares up the pulses, and retransmits the signals onto the line to the receiving station. Because the original transmitted signal is restored (squared up), the communication system becomes less susceptible to noise and other types of interference on the lines.

The shown "use of repeaters" application for bidirectional control of an RS-485 bus with long transmission lines is implemented with a bidirectional repeater station. Two types of repeaters are available: One version is enabled by a logic 1 control signal and the other by a logic 0. Thus, without any glue logic you can design a fully bidirectional repeater station that restores signals from both directions on a line

Enabling and disabling of the repeater drivers and receivers and thereby the data direction is controlled by the host microcontroller. In data communication systems where no host CPU controls the data direction, intelligence needs to build into the repeater station to maintain system control. This allows also for independent communication on each side of the repeater station providing additional flexibility and faster overall data exchange.

Recommended Products

Dedicated products designed specifically for repeater purposes are the SN75177B and SN75178B. Employing these repeater devices in simple repeater stations as the shown, completely eliminates the need for any glue logic due to their enabling scheme. For repeater stations including protocol controllers may also benefit from devices such as SN751177 and SN1178 with their multiple drivers and receivers.

Notes

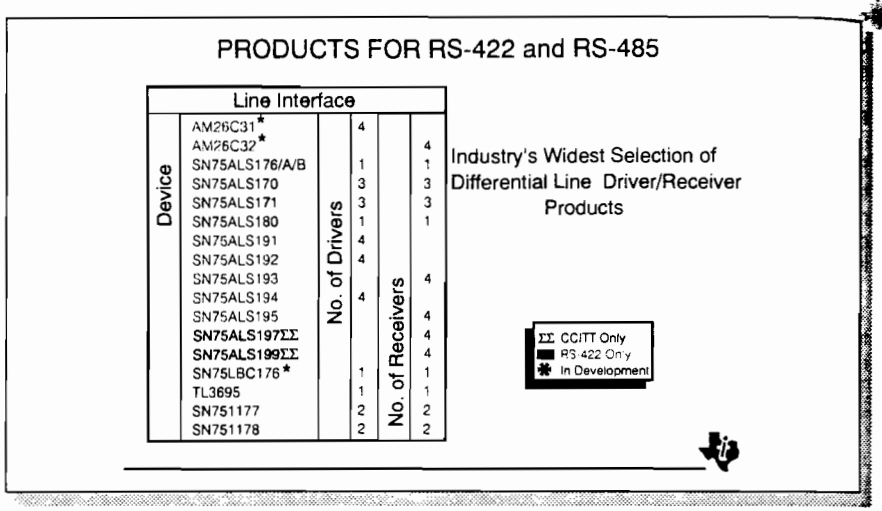


Figure 23 - New Products For RS-422 and RS-485

The figure shows the range of devices available for the EIA RS-422 and RS-485 standards. Of particular note is the trend towards devices combining low-power and high-speed capabilities which also offer a variety of enablling schemes and multiple driver/receiver combinations. Also of note are the SN75ALS170, SN75ALS171 and SN75LBC176, these are the subjects of the following section.

The ANSI Small Computer Systems Interface